AMENDMENTS TO THE CLAIMS

Please amend claims 55, 58-59, 62-63, 66-69, 71, 74-75, 78, and 81 as indicated below. Please add new claims 85-89.

Claims 1-54 (Cancelled)

55. (Currently Amended) A system comprising:

a connector to ~~couple the system to~~ a bus;

an instruction memory to store a plurality of bus stimuli instructions that represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases; and

one or more phase generators coupled between the instruction memory and the connector, the one or more phase generators to receive the plurality of bus stimuli instructions from the instruction memory and to provide a plurality of signals on the bus that represent the predefined sequence of bus transactions.

56. (Previously Added) The system of claim 55, wherein the predefined sequence of bus transactions comprises a user specified sequence of bus transactions that has been specified by a user in a high level language.

57. (Previously Added) The system of claim 55, wherein the predefined sequence of bus transactions comprises an illegal sequence of bus transactions.

58. (Currently Amended) The system of claim 55, wherein the predefined sequence of bus transactions is based on ~~a pre-existing~~ an existing simulation stimulus software.

59. (Currently Amended) The system of claim 55, wherein the predefined sequence of bus transactions is the same as a corresponding predefined sequence of bus transactions specified in ~~a pre-existing~~ an existing simulation stimulus software.

60. (Previously Added) The system of claim 55, wherein an instruction of the plurality of bus stimuli instructions comprises an instruction word having a predefined length, the instruction word containing a plurality of predefined segments, each of the plurality of segments to provide instruction to a different portion of the one or more phase generators.

61. (Previously Added) The system of claim 55:

wherein an instruction of the plurality of bus stimuli instructions comprises an instruction word having a predefined length, the instruction word having a plurality of predefined segments; and

wherein a first segment of the plurality of predefined segments contains a type of operation, a second segment of the plurality of predefined segments contains an arbitration instruction, a third segment of the plurality of predefined segments contains address and transaction data, and a fourth segment of the plurality of predefined segments contains a data memory address.

62. (Currently Amended) The system of claim 55, further comprising ~~a connection~~ an interface to a computer ~~system, in which the instruction memory and the one or more phase generators are not implemented,~~ to receive the plurality of predefined bus stimuli instructions.

63. (Currently Amended) The system of claim 55:

wherein the one or more phase generators includes at least one digital logic device coupled with the instruction memory to generate digital logic representing the

plurality of bus stimuli instructions, and at least one phase engine coupled

between the digital logic device and the connector to translate the digital logic

into the plurality of signals and to time providing the signals to the bus, ~~the at~~

~~least one digital logic device to generate digital logic representing the plurality of~~

~~bus stimuli instructions and to provide the digital logic to the at least one phase~~

~~engine, the at least one phase engine to translate the received digital logic into the~~

~~plurality of signals and to time providing the signals to the bus~~; and

further comprising a response memory coupled with the at least one digital logic

device to store information relating to a bus transaction phase and a response to a

bus stimuli.

64.   (Previously Added) The system of claim 63:

wherein the connector comprises a connector to connect with a processor socket

on a motherboard;

wherein the instruction memory comprises a static random access memory;

wherein the at least one digital logic device comprises a device selected from the

group consisting of a field programmable gate array and an application specific

integrated circuit; and

wherein the at least one phase engine comprises a logic level translation device.

65.   (Previously Added) The system of claim 63:

wherein the at least one digital logic device comprises a control logic portion to

control phases of a bus transaction including to conduct an arbitration phase and a

request phase of the bus transaction, and a data logic portion to exchange data

with a bus agent coupled with the bus according to the bus transaction;

further comprising a response memory coupled with the control logic portion to store information relating to a bus transaction phase and a response to a bus stimuli;

further comprising a data memory coupled with the data logic portion to store the exchanged data; and

wherein the at least one phase engine comprises a control phase engine coupled with the control logic portion and a data phase engine coupled with the data logic portion, the control phase engine and the data phase engine to time providing the plurality of signals on the bus.

66.   (Currently Amended) A system comprising:

a connector to ~~couple the system to~~ a bus;

an instruction memory to store a bus stimuli instruction, the instruction having a predefined length, the instruction containing a plurality of segments, the plurality of segments including at least a flow segment and a data segment;

a logic device <u>coupled with the instruction memory to receive the bus stimuli instruction and generate digital logic based on the bus stimuli instruction, the logic device</u> comprising a flow portion, a request portion, and a data portion ~~that are each coupled with the instruction memory to receive at least a segment of the bus stimuli instruction~~, the flow portion to receive at least the flow segment from the instruction memory, and the data portion to receive at least the data segment from the <u>instruction</u> memory, the flow portion, the request portion, and the data portion each comprising a device selected from the group consisting of a field programmable gate array and an application specific integrated circuit~~, the device to generate digital logic according to the bus stimuli instruction~~;

a plurality of phase engines <u>coupled between the logic device and the connector to translate the digital logic into signals and provide the signals to the bus, the plurality of phase engines</u> including a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine ~~coupled between the logic device and the connector~~, the system phase engine, the arbitration phase engine, and the request phase engine coupled with the flow portion, the snoop/error phase engine coupled with the request portion, the data phase engine coupled with the data portion~~, the plurality of phase engines to translate the digital logic received from the logic device into signals and to provide the signals to the bus~~;

further comprising a response memory coupled with the flow portion and the request portion to store response information; and

further comprising a data memory coupled with the data portion to store data.

67.   (Currently Amended) The system of claim 66, further comprising ~~a connection~~ <u>an</u> interface to a computer ~~system, in which the instruction memory is not implemented,~~ to receive the bus stimuli instruction.

68.   (Currently Amended) The system of claim 66, wherein the bus stimuli instruction is based on ~~a pre-existing~~ <u>an existing</u> simulation stimulus software.

69.   (Currently Amended) A system comprising:

a computer ~~system~~ containing a file that is based on ~~a pre-existing~~ <u>an existing</u> simulation stimulus software and that contains a plurality of bus stimuli instructions that represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases;

a processor bus;

a transaction generator ~~contai~~ning a first connector coupled to the computer to receive the file and containing a second connector coupled to the bus to provide a plurality of bus compatible signals to the bus, ~~coupled between the computer system and the bus,~~ the transaction generator further containing:

~~a first connector coupled to the computer system to receive the file;~~

an instruction memory to store the file; and

one or more phase generators coupled ~~between~~ with the instruction memory ~~and the first connector, the one or more phase generators~~ to receive the plurality of bus stimuli instructions ~~from the file stored in the instruction memory~~ and to generate ~~a~~ the plurality of bus compatible signals that represent the predefined sequence of bus transactions,

wherein the one or more phase generators include a logic device selected from the group consisting of a flow programmable gate array and an application specific integrated circuit ~~coupled with the instruction memory~~ to implement the instructions as digital logic, and

wherein the one or more phase generators include a translation device coupled between the logic device and the bus to translate the digital logic to the plurality of bus compatible signals; and

~~a second connector coupled to the bus to provide the plurality of bus compatible signals to the bus; and~~

a component selected from the group consisting of a processor and a chipset coupled ~~attached~~ to the bus to respond to the plurality of bus compatible signals.

70.   (Previously Added) The system of claim 69, further comprising a logic analyzer coupled with the bus to capture information associated with the response of the component to the plurality of bus compatible signals.

71.   (Currently Amended) The system of claim 69, wherein the plurality of bus stimuli instructions ~~comprise~~ are based on a high level language.

72.   (Previously Added) A system comprising:

an instruction memory to store a plurality of instructions representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases; and

phase generator means for implementing the plurality of instructions on the bus as the predefined sequence of bus transactions.

73.   (Previously Added) The system of claim 72, wherein the phase generator means comprises:

logic device means for generating digital logic based on the instructions; and

phase engine means for translating the digital logic into bus logic.

74.   (Currently Amended) The system of claim 72, contained within a second system comprising a computer ~~system~~ coupled with the instruction memory, a bus coupled with the phase generator means, and a component coupled with the bus, ~~wherein the computer system contains a file containing the plurality of instructions, and wherein the component is selected from the group consisting of a processor and a chipset.~~

75. (Currently Amended) A method comprising:

coupling a component to a bus;

coupling a device comprising an instruction memory and a phase generator to the bus;

storing a plurality of instructions representing a predefined sequence of bus transactions in the instruction memory;

providing the plurality of instructions from the instruction memory to the phase generator;

using the phase generator to provide signals representing the predefined sequence of bus transactions to the bus based on ~~according to~~ the plurality of instructions; and

detecting a bug of the component by determining an incorrect response of the component to the predefined sequence of bus transactions.

76. (Previously Added) A component designed to eliminate a bug detected by the method of claim 75, wherein the component comprises a processor.

77. (Previously Added) A component designed to eliminate a bug detected by the method of claim 75, wherein the component comprises a chipset.

78. (Currently Amended) The method of claim 75, further comprising ~~generating~~ specifying the plurality of instructions ~~representing the predefined sequence of bus transactions~~ in a high level language ~~based on a simulation stimulus software~~.

Claims 79-84 (Cancelled)

85.   (New) A method comprising:

specifying a sequence of bus transactions;

assembling the sequence into a file;

providing the file to a memory of a bus transaction generator;

implementing the predefined sequence of bus transactions on a bus using a phase generator of the bus transaction generator; and

capturing a response to the predetermined sequence of bus transactions.

86.   (New) The method of claim 85, wherein assembling the sequence into a file comprises assembling the sequence into a binary object file.

87.   (New) The method of claim 85, wherein specifying the sequence of bus transactions comprises specifying a sequence of bus transactions in a high level language.

88.   (New) The method of claim 85, wherein capturing the response comprises capturing an incorrect response to a legal sequence of bus transactions.

89.   (New) The method of claim 85, wherein capturing the response comprises detecting a bug.